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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/702,448	11/07/2003	Toru Ichien	XA-9957	9708

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/702,448	ICHIEN ET AL.	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 21-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-14,21-26,28-30,32 and 36* is/are rejected.

7)☒ Claim(s) *8-10,15-17,27,31 and 33-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/7/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-17 and 21-36 in the reply filed on 7/26/06 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 11-14, 21-26, 28-30, 32 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al., US Patent no. 6,467,042 [Wright] and Yen, US Patent no. 6,744,634, in view of Uzelac, US Patent no. 6,611,918.

Regarding claim 1, Wright discloses a semiconductor data processing device for connecting to a general-purpose bus [USB] of a host system, in which said data processing device enters an active state or standby state in response to a state of said general-purpose bus, said data processing device comprising:

a clock circuit [SUSPEND/SLEEP CONTROLLER in Figure 2] for stopping an internal clock signal in said standby state [column 2, lines 35-38 and column 3, lines 15-25].

Wright discloses that the data processing device is a USB peripheral device, but is silent as to the specific function of the device. Yen discloses a well known USB memory card device [Figure 9 and column 5, lines 15-32]. It would have been obvious to one of ordainry skill in the art to use a well known USB memory card device as the USB device in the Wright teachings.

Wright and Yen do not disclose a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current in said standby state. Uzelac discloses a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current when a circuit is operating in a standby state [column 2, lines 10-28]. It would have been obvious to one of ordinary skill in the art to include voltage generation circuitry for applying a substrate bias voltage in a direction for reducing a threshold leak current when the Wright and Yen device is operating in a standby state in order to reduce unnecessary power consumption [Uzelac, column 1, lines 20-31].

Regarding claims 2 and 11, Yen further discloses a rewritable non-volatile memory [Memory Components in Figure 9] for storing a control program for connecting said non-volatile storage device to said general-purpose bus; and a central processing unit for executing said control program [controller, column 5, lines 9-14].

Regarding claim 3, Wright further discloses a circuit for detecting the state of said general-purpose bus to control state changes from said standby state to said active state [TRAFFIC DETECT in Figure 2 and column 3, lines 21-29].

Regarding claim 4, Yen further discloses a first interface controller that interfaces with said non-volatile storage device [Memory Card Interface in Figure 9].

Regarding claim 5, Yen further discloses a second interface controller that interfaces with said general-purpose bus [USB Interface in Figure 9].

Regarding claim 6, Yen further discloses that the first interface controller is a memory card interface controller and said second interface controller is a USB interface controller [Figure 9].

Regarding claims 7, 12-14 and 32, Yen further discloses a data transfer controller for controlling data transfer between said first interface controller and said second interface controller [controller, column 5, lines 9-14].

Regarding claims 21and 22, Wright discloses a data processing system comprising a circuit for connecting a device to a general-purpose bus [USB],

wherein said semiconductor data processing device changes its state from active to standby in response to the state of said general-purpose bus and stops an internal clock signal [column 2, lines 35-38 and column 3, lines 15-25].

Wright discloses that the data processing device is a USB peripheral device, but is silent as to the specific function of the device. Yen discloses a well known USB to memory card bridge device [Figure 9 and column 5, lines 15-32]. Yen further discloses a rewritable non-volatile memory [Memory Components in Figure 9] for storing a control program for connecting a non-volatile storage device to said general-purpose bus and a central processing unit for executing said control program [controller, column 5, lines 9-14]. It would have been obvious to one of ordinary skill in the art to use a well known USB memory card bridge device as the USB device in the Wright teachings.

Wright and Yen do not disclose a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current in said standby state. Uzelac discloses a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current when a circuit is operating in a standby state [column 2, lines 10-28]. It would have been obvious to one of ordinary skill in the art to include voltage generation circuitry for applying a substrate bias voltage in a direction for reducing a threshold leak current when the Wright and Yen device is operating in a standby state in order to reduce unnecessary power consumption [Uzelac, column 1, lines 20-31].

Regarding claims 23 and 36, Wright further discloses an idle state and a communication request state [column 4, lines 20-30].

Regarding claim 24, Wright discloses a semiconductor data processing device, comprising:

a clock generation circuit [CLOCK GENERATOR in Figure 2];

a first control circuit [SUSPEND/SLEEP Controller];

wherein said clock generation circuit stops generation of said clock when said data processing device enters said standby state [column 2, lines 35-38 and column 3, lines 15-25].

Wright discloses that the data processing device is a USB peripheral device, but is silent as to the specific function of the device. Yen discloses a well known USB memory card bridge device [Figure 9 and column 5, lines 15-32]. Yen further discloses a rewritable non-volatile memory [Memory Components in Figure 9] for storing a control program for connecting a non-volatile storage device to said general-purpose bus and a central processing unit for executing said control program [controller, column 5, lines 9-14]. It would have been obvious to one of

ordinary skill in the art to use a well known USB memory card bridge device as the USB device in the Wright teachings.

Wright and Yen do not disclose a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current in said standby state. Uzelac discloses a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current when a circuit is operating in a standby state [column 2, lines 10-28]. It would have been obvious to one of ordinary skill in the art to include voltage generation circuitry for applying a substrate bias voltage in a direction for reducing a threshold leak current when the Wright and Yen device is operating in a standby state in order to reduce unnecessary power consumption [Uzelac, column 1, lines 20-31].

Regarding claim 25, Wright further discloses that the first control circuit receives first and second supply potentials to be driven to operate regardless of whether said data processing device is in said standby state or not [column 4, line 67 – column 5, line 1].

Regarding claim 26, Wright further discloses a first detection circuit for detecting the state of a bus to which it is be connected [TRAFFIC DETECT in Figure 2 and column 3, lines 21-29], wherein said first control circuit controls the elements of said peripheral circuit except for said first detection circuit in response to said standby state, and wherein said first detection circuit receives first and second supply potentials to be driven to operate regardless of whether or not said data processing device is in said stand-by state [Figure 2, column 3, lines 21-25 and column 4, lines 64-66].

Regarding claim 28, Regarding claims 21-23, Wright discloses a data processing system comprising a circuit for connecting a device to a general-purpose bus [USB],

a clock generation circuit [CLOCK GENERATOR in Figure 2];

a first control circuit [SUSPEND/SLEEP Controller];

wherein said clock generation circuit stops generation of said clock when said data processing device enters said standby state [column 2, lines 35-38 and column 3, lines 15-25].

wherein said semiconductor data processing device changes its state from active to standby in response to the first state of said general-purpose bus and stops an internal clock signal [column 2, lines 35-38 and column 3, lines 15-25]; and

wherein said semiconductor data processing device changes the state from said standby to said active in response to the second state of said general-purpose bus, said second state following said first state [column 4, lines 20-30].

Wright discloses that the data processing device is a USB peripheral device, but is silent as to the specific function of the device. Yen discloses a well known USB to memory card bridge device [Figure 9 and column 5, lines 15-32]. Yen further discloses a rewritable non-volatile memory [Memory Components in Figure 9] for storing a control program for connecting a non-volatile storage device to said general-purpose bus and a central processing unit for executing said control program [controller, column 5, lines 9-14]. It would have been obvious to one of ordinary skill in the art to use a well known USB memory card bridge device as the USB device in the Wright teachings.

Wright and Yen do not disclose a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current in said standby state. Uzelac discloses a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current when a circuit is operating in a standby state [column 2, lines

10-28]. It would have been obvious to one of ordinary skill in the art to include voltage generation circuitry for applying a substrate bias voltage in a direction for reducing a threshold leak current when the Wright and Yen device is operating in a standby state in order to reduce unnecessary power consumption [Uzelac, column 1, lines 20-31].

Regarding claim 29, Wright further discloses that the first control circuit receives first and second supply potentials to be driven to operate regardless of whether said data processing device is in said standby state or not [column 4, line 67 – column 5, line 1].

Regarding claim 30, Wright further discloses a first detection circuit for detecting the state of a bus to which it is be connected [TRAFFIC DETECT in Figure 2 and column 3, lines 21-29], wherein said first control circuit controls the elements of said peripheral circuit except for said first detection circuit in response to said standby state, and wherein said first detection circuit receives first and second supply potentials to be driven to operate regardless of whether or not said data processing device is in said stand-by state [Figure 2, column 3, lines 21-25 and column 4, lines 64-66].

Allowable Subject Matter

Claims 8-10, 15-17, 27, 31 and 33-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Teng et al., US Patent Application Publication no. 2003/0178486, discloses a USB memory card reader.

Wright et al., US Patent no. 6,816,976 discloses a system and method for reducing power consumption in a USB device.

Jackson et al., US Patent no. 6,085,325 discloses a method and apparatus for power conservation modes in a bus-powered device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Yanchus
October 16, 2006

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